## IN THE DRAWINGS

Please replace sheet 2 with the attached replacement sheet 2.

## REMARKS

Claims 1-44 are pending in the present application. In the above amendments, claims 9 and 14-16 have been amended, claims 17-29 and 38-44 have been withdrawn, and new claims 45-55 have been added. Therefore, after entry of the above amendments, claims 1-16, 30-37, and 45-55 will be pending in this application. Applicant believes that the present application is now in condition for allowance, which prompt and favorable action is respectfully requested.

**The Specification**

Paragraphs [1032], [1074] and [1085] have been amended to correct typographical errors. No new matter has been introduced.

**The Drawings**

FIG. 3 in sheet 2 has been amended to match the Specification. The clock input of latch 316a has been changed from S2 to S2b, and the clock input of latch 316b has been changed from S1 to S1b, as indicated in paragraph [1032].

**Election/Restrictions**

In view of the restriction requirement, Applicant elects to prosecute the invention of Group I, claims 1-16 and 30-37. Claims 17-29 and 38-44 have been withdrawn in response to the restriction requirement.

**Allowed Claims 1-8 and 30-35**

Applicant notes with appreciation the allowance of claim 1-8 and 30-35.

**Objected to Claim 14**

Claim 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 14 has been amended to include all of the limitations of base claim 9 and intervening claim 13. Applicant submits that claim 14 is now allowable.

**Rejection of Claims 9-13, 15, 16, 36 and 37 Under 35 U.S.C. §102(b)**

Claims 9-13, 15, 16, 36 and 37 stand rejected under 35 U.S.C. §102(b) as being anticipated by Gillig *et al* (U.S. Patent No. 5,703,539). The rejection indicates that Gillig teaches all of the limitations of these claims.

Gillig describes an apparatus and method for controlling the loop bandwidth of a phase locked loop (PLL) **308**. An edge proximity detector **302** receives a reference frequency signal at line **206** and a feedback signal at line **209** and identifies a phase error between the two signals as either desirable or undesirable. When the phase error is identified as desirable, a counter **301** determines a rate of change of the phase error over a first predetermined time period to provide an indication of frequency error between the frequency of the reference frequency signal and the frequency of the output frequency signal. A loop bandwidth adjuster **310** controls a transition between a first and a second loop bandwidth state of the PLL **308** responsive to the indication of the frequency error. (See the Abstract.)

Independent claim 9 of the present invention, as amended, recites:

> "An integrated circuit comprising:
>
> a phase-frequency detector (PFD) operative to receive a reference signal and a feedback signal, compare phase of the reference signal against phase of the feedback signal, and provide a detector output comprised of a sequence of phase error values, each phase error value indicating whether the phase of the reference signal is early or late with respect to the phase of the feedback signal; and
>
> a loop filter (LF) operative to receive and filter the detector output and provide an LF output, wherein the loop filter is operative to adjust loop bandwidth of a digital phase-locked loop (PLL) based on the sequence of phase error values from the phase-frequency detector."

Applicant submits that claim 9 is not anticipated by Gillig. In particular, Gillig does not describe "the loop filter is operative to adjust loop bandwidth of a digital phase-locked loop (PLL) based on the sequence of phase error values from the phase-frequency detector," as claim 9 recites. In Gillig, a loop bandwidth controller **300** receives a reference frequency signal at line **206** and a feedback signal at line **209** and produces a loop bandwidth adjust signal at line **309**. Loop bandwidth controller **300** does not receive nor use the output of phase detector **202** for loop bandwidth adjustment, as claim 9 recites. In fact, Gillig teaches away from using the output of phase detector **202** to adjust the loop bandwidth. Gillig states "digital processing of the phase error signal at line **207** is difficult to achieve when the phase

error at line 207 is small, i.e. when the PLL 308 is close to lock." (See column 6, lines 41-44.)

For at least the above reasons, Applicant submits that claim 9 is not anticipated by Gillig. Claims 10-13 are dependent on claim 9 and are not anticipated by Gillig for at least the reasons noted for base claim 9. These dependent claims may recite additional features not described nor suggested by Gillig.

For claim 11, Gillig does not describe "increase the loop bandwidth if a large phase error between the reference and feedback signals is detected." Rather, Gillig identifies a phase error as being either desirable or undesirable and, if desirable, determines a rate of change of the phase error to provide an indication of frequency error. Gillig then adjusts the bandwidth based on the frequency error.

For claim 12, Gillig does not describe "the large phase error is detected if a particular number of consecutive phase error values with same polarity are received." Gillig does not describe detecting for a large phase error, as noted above for claim 11, and hence does not describe how to detect this large phase error.

For claim 13, Gillig does not describe "decrease the loop bandwidth if a small average phase error is detected." Rather, Gillig detects for frequency error, as noted above.

Independent claims 36 and 37 each recite features not described by Gillig and are thus not anticipated by Gillig. For example, claims 36 and 37 recite "detecting for a large phase error in the detector output" and "detecting for a small average phase error in the detector output". As noted above, Gillig identifies whether the phase error is desirable or undesirable and, if desirable, detects frequency error and adjusts the loop bandwidth based on the frequency error.

Accordingly, the §102(b) rejection of claims 9-13, 15, 16, 36 and 37 should be withdrawn.

**New Claims**

New claims 45-55 recited additional features of the invention. Claims 45-48 are dependent on allowed claim 1, claims 49-50 are dependent on allowed claim 7, claims 51-52 are dependent on allowed claim 8, and claims 53-55 are dependent on allowed claim 30. These new claims are thus allowable. Support for claims 45 and 46 is given in paragraph [1042], support for claim 47 is given in paragraph [1050], support for claims 48, 50 and 52 is

given in paragraph [1045], support for claims 49 and 51 is given in paragraph [1046], support for claim 53 is given in paragraph [1055], and support for claims 54 and 55 is given in paragraphs [1061] and [1062].

## CONCLUSION

In light of the amendments contained herein, Applicant submits that the application is in condition for allowance, for which early action is requested.

Please charge any fees or overpayments that may be due with this response to Deposit Account No. 17-0026.

Respectfully submitted,

Dated: 9/13/05

By: _____
George C. Pappas, Reg. No. 35,065
858-651-1306

QUALCOMM Incorporated
Attn: Patent Department
5775 Morehouse Drive
San Diego, California 92121-1714
Telephone: (858) 658-5787
Facsimile: (858) 658-2502